REMARKS

Applicant initially would like to thank the Examiner for the recognition of allowable subject matter as set forth in claims 52-54, as well as the recognition of claims 9-12, 45-47, 49-51 and 55 would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Further, Applicant notes that claims 4, 18-23, 38 and 43 were not objected to by the Examiner, as each claim variously contains one or more patentable elements set forth in paragraph 11 of the Examiner's statement of reasons for the indication of allowable subject matter.

In the May 28, 2004 Office Action, the Examiner rejected claims 1-3, 5, 6-8, 13-17, 24-37, 39-42, 44, 48 and 56-59, objected to claims 9-12, 45-47, 49-51 and 55, and allowed claims 52-54. The present amendment and response amends claims 1, 5, 7 and 8. After entry of this amendment, claims 1-59 remain pending in the application. No new subject matter is being added by these amendments. Support for the amendments to the claims can be found generally in paragraphs 8, 25 and 26 of the specification. In view of the foregoing remarks, reconsideration of the application is respectfully requested.

Claim Rejections

Claims 1, 5, 7 and 8 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Keeth, U.S. Patent No. 5,872,736 ("Keeth"). In particular, the Examiner relied on Figure 9 of Keeth in an attempt to illustrate anticipation of each and every element of the claims. Applicant respectfully traverses these rejections.

Keeth generally discloses an output driver circuit 200 having optional slew rate control circuits 210, a pull-up drive adjust circuit 214 and a pull-down drive adjust circuit 216. A pull-up transistor 206 and a pull-down transistor 208 have their control terminals coupled to the slew rate control circuits 210. The purpose of the output driver circuit 200 is to adjust control circuits 210 using V_{SLEW} signals to selectively activate a series of transistors 218, i.e., by selectively activating any of the transistors 218, a parallel resistor 220 is bypassed, and thereto change the response time of the circuit. Stated another way, the gates of transistors 218 are selectively activated to bypass resistors 220 to change the response time of the circuit.

The signals V_{TRIM} 1-6 are not originated from variable power supply voltage, but instead comprise a control signal designed to "turn on" transistors 218 to bypass resistors 220. Thus, any changes to a power supply (for example, changes to a supply coupled to the source of the upper transistor 218) do not change the slew rate of the output driver circuit 200. Instead, the slew rate is changed by turning on one or more transistors 218.

Applicant's independent claim 1 recites an output buffer configured for use within DRAM applications, said output buffer comprising an output driver circuit configured for providing an output signal for said output buffer, and a slew rate control circuit coupled to said output driver circuit and configured for receiving a drive input signal and for

controlling a slew rate of said drive input signal based on a level of voltage provided from a power supply to said output driver circuit, wherein increases in said level of voltage decrease said slew rate and decreases in said level of voltage increase said slew rate.

In sharp contrast to Keeth, claim 1 is configured such that increases in the level of the power supply (V_{CCQ}) operate to increase or decrease the slew rate (for example, see paragraphs 25 and 26 of Applicant's specification). Keeth does not teach a technique for adjustment of the slew rate. Accordingly, Applicant's claim 1 is not taught or suggested by Keeth.

Applicant's independent 5 recites the output buffer according to claim 1, wherein said output driver circuit comprises a pull-up transistor having an input terminal connected to the power supply, and a control terminal coupled to said slew rate control circuit, and a pull-down transistor having an input terminal connected to a ground connection, an output terminal coupled to an output terminal of said pull-up transistor, and a control terminal coupled to said slew rate control circuit. Keeth does not disclose or suggest a pull-up transistor having an input terminal, for example, a source connected to the power supply, and a pull-down transistor having an input terminal (source) "connected" to a ground connection. In contrast, the pull-up transistor 206 of Keeth has a source coupled to transistors 218 and transistors 220 and a pull-down transistor 208 having a source connected to transistors 218 and 220. The purpose of transistors 218, 220 is for selectively bypassing resistor 220 to change response time, as opposed to controlling the slew rate based on the level of supply voltage V_{CCQ}. Accordingly, claim 5 is also not taught or suggested by Keeth.

Likewise, Applicant's independent claim 7 recites an output buffer configured for use in memory applications, said output buffer comprising an output driver circuit configured for providing an output signal for said output buffer, wherein said output driver circuit comprises a pull-up transistor having an input terminal connected to a power supply, and a pull-down transistor having an input terminal connected to a ground connection, an output terminal coupled to an output terminal of said pull-up transistor, and a slew rate control circuit coupled to control terminals of said pull-up transistor and said pull-down transistor of said output driver circuit and configured for controlling a slew rate of a drive input signal. For reasons discussed above in claim 5, each and every element of claim 7 is also not taught or suggested by Keeth.

Finally, claim 8 recites the output buffer according to claim 7, wherein said slew rate control circuit is configured for controlling a slew rate of a drive input signal based on a level of voltage in said power supply provided to said output driver circuit, wherein increases in said level of voltage decrease said slew rate and decreases in said level of voltage increase said slew rate. Again, similar to claims 5 and 7, each and every element is not disclosed by Keeth.

Accordingly, Applicant respectfully submits that each and every element of independent claims 1, 5, 7 and 8 are not disclosed, taught or suggested by Keeth. Thus, claims 1, 5, 7 and 8 are not anticipated by Keeth, and Applicant respectfully requests the withdrawal of the rejections of those claims under 35 U.S.C. § 102(b).

Claims 1-3, 6, 13-17, 24-37, 39-42, 44, 48, and 56-59 stand rejected under judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1, 2, 4, 14-28, 31-33, 41, 42, and 44 of U.S. Patent No. 6,714,462 ('462).

While Applicant respectfully disagrees with these double patenting rejections, in the interest of compact prosecution, Applicant respectfully submits a terminal disclaimer, without prejudice, in compliance with 37 CFR 1.321(c) in that the nonstatuatory double patenting rejections are based on the '462 patent which is commonly owned with the patent application by Assignee Micron Technology, Inc.

CONCLUSION

In view of the foregoing, Applicant respectfully requests withdrawal of the § 102 rejections to claims 1, 5, 7 and 8 and the issuance of a notice of allowance for pending claims. Should the Examiner wish to discuss any of the above in greater detail or deem that further amendments should be made to improve the form of the claims, then the Examiner is invited to telephone the undersigned at the Examiner's convenience.

Respectfully submitted,

Date: 7/23/04

By: _____
R. Lee Fraley, Reg. No. 42,550

SNELL & WILMER, L.L.P.
One Arizona Center
400 East Van Buren
Phoenix, AZ 85004-2202
(602) 382-6250